System technology co-optimization for high speed/high frequency chiplets and heterogeneous integration packaging
Leuven |

Are you ready to embark on an exciting journey into the cutting-edge world of semiconductors? Today, the semiconductor industry is undergoing a profound transformation, and we invite you to be part of it.

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Imagine a future where electronics are more powerful, energy-efficient, sustainable, and flexible than ever before. This is the promise of chiplets.
Chiplets are a disruptive technology, where a monolithic chip is deconstructed into modular functional blocks or chiplets and then cleverly reassemble at the packaging level connecting the different chiplets.This LEGO-like approach marks a new era of semiconductor innovation because it promises to reduce chipmaking costs by enabling the production of different functional circuits using the most cost-effective processes.
However, because they're developed independently by different manufacturers, chiplet products are often not interoperable and compatible, resulting in a fragmented chiplet ecosystem. Moreover, while chiplet and packaging technologies work hand in hand to redefine the possibilities of chip integration, this technological tie-up isn't simple and straightforward. To fulfil the potential of chiplets and enable efficient system integration, heterogenous integration of chiplet-based systems become even more important. Furthermore, while chiplets have made significant strides in digital and memory applications, there is still substantial research needed in RF and analog applications like wireless communication.
That's where you come in. This PhD topic focuses on a crucial aspect of this revolution – system-technology co-optimization. Today, interconnects have become major bottlenecks for the chiplet concept and therefore, the improvement of interconnect speed is essential for chiplet-based system performance. However, higher speed interconnects typically also entail higher losses and therefore, system-wide optimization is required.

In this PhD project, you'll collaborate with 3D technologists and RF design experts to tackle these challenges head-on. You'll work on the design aspects of co-optimizing chiplet-based systems for peak performance and delve into the details of heterogeneous integration technology.
Specifically, the work will entail:

- Literature review and benchmarking the state of the art.
- Minimization of the (ever increasing) number of interconnect lines between chiplets by extending interconnects to higher frequencies
- Development of low RF loss interconnects by
    - fab and chiplets compatible new conductors
    - fab and chiplets compatible new dielectrics
    - design methodology optimization
- Modelling and design of microwave properties using different packaging techniques of
    - high speed/high frequency interconnects

- chiplet-based systems to benchmark their performance.

You will work at imec across different departments and teams in a world-class R&D environment. Your daily advisor will be an IMEC principal scientist Dr. Xiao Sun. Your PhD supervisor will be prof. Dr. Nadine Collaert from the Vrije Universiteit Brussel

Required background: Electrical Engineering, Microelectronics, RF and microwave
Type of work: 40 simulation/modeling, 20% design, 10% characterization, 10% literature
Supervisor: Nadine Collaert
Co-supervisor: Xiao Sun
Daily advisor: Xiao Sun
The reference code for this position is **2025-019**. Mention this reference code on your application form.